Group A: Hardware Acceleration for Machine Learning

Number	Title	Authors	Affilication
1	Energy-efficient approximated feedforward neural network accelerator	D. Kim, S. Mukhopadhyay	GaTech
2	Energy efficient system design for neural networks	B. Li, Y. Wang, H. Yang	Tsinghua
3	Adaptive precision control in digital cellular neural network	J. Kung, S. Mukhopadhyay	GaTech
4	Reducing deep neural network complexity for low-power applications through parameter ranking	M. Tu, V. Berisha, M. Woolf, J. Seo, Y. Cao	ASU
5	A hardware accelerator for convolutional neural networks	V. Gokhale, E. Culurciello	Purdue
6	Distributed acceleration of sequential minimal optimization on FPGAs	J. Tai, I. Ahmed, P. Wu, V. Betz, P. Chow	U. Toronto
7	Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile	K. Ma, X. Li, Y. Liu, J. Sampson, Y. Xie, V. Narayanan	PSU
8	Exploring the design space of GPGPUs for deep learning acceleration	M. Zhu, Z. Qi, C. Wang, Y. Xie	UCSB
9	Dot-product engine for deep learning	M. Hu	HP
10	An FPGA-based hardware accelerator for real-time traffic sign detection	W. Shi, X. Li, G. Overett, Z. Yu	CMU
11	Real-time face detection with CPU-FPGA acceleration	A. Mohanty, M. Kim, N. Suda, S. Vrudhula, J. Seo, Y. Cao	ASU
12	A HW/SW implementation of a handwritten digit recognition system based on convolutional neural network	L. B. Saldanha, C. Bobda	U. Arkansas
13	Design and optimization of energy-efficient cascaded classifiers on silicon	A. Wang, W. Xu	SUNY, Buffalo
14	Sampling and graph cut based probabilistic inference architectures for machine learning tasks	G. G. Ko, T. Gao, R. A. Rutenbar	UIUC
15	Embedded algorithmic noise tolerance for signal processing and machine learning	S. Zhang, N. Shanbhag	UIUC

Group B: Neuromorphic Computing and Applications

Number	Title	Authors	Affilication
16	Conquering MPSoC complexity with bio-inspired self-organization	A. Herkersdorf, W. Rosenstiel, A. Oeldemann, P. Wagner, T. Wild	TUM
17	Analyzing server hardware monitors for statistical learning chip	B. Osbun, S. Blanton, D. Thomas	CMU
18	Learning based compact thermal modeling for energy-efficient smart building management	H. Zhao, S. Wang, X. Li, S. X.-D. Tan	UC Riverside
19	Learning for VMM + WTA embedded classifiers	S. Shah, J. Hasler	GaTech
20	Synaptic sampling with the neural and synaptic array transceiver	S. Sheik, S. Paul, C. Augustine, C. Kothapalli, G. Cauweberghs, E. Neftci	UC Irvine
21	An experimentation platform for on-chip integration of analog neural networks: a pathway to trusted and robust analog/RF ICs	D. Maliuk, G. Volanis, Y. Makris	UT Dallas
22	Combination of supervised and unsupervised learning in network of biological spiking neurons	S. Skorheim, P. Sanda, M. Bazhenov	UC Riverside
23	Sparse learning with reward, habituation, inhibition and noise	Z. Xu, S. Skorheim, M. Bazhenov, J. Seo, S. Yu, Y. Cao	ASU
24	Neuromorphic computing system for machine learning	B. Liu, Y. Chen	U. Pittsburgh
25	Spiking neuromorphic systems with nanoelectronic synapses for online learning	S. B. Eryilmaz, S. Joshi, G. Cauwenberghs, H.-S. P. Wong	Stanford
26	A morphable process-in-memory architecture for neural computation in ReRAM-based main memory	S. Li, P. Chi, Y. Xie	UCSB
27	Design of stochastic feed forward networks with memristive primitives	D. Christiani, C. Merkel, D. Kudithipudi	RIT
28	Multi-bit storage and pattern recognition with the aid of memristor	S. Manoj P. D., N. Taherinejad, A. Jantsch	TUWien
29	Neuromorphic architecture inspired fast, efficient and configurable on-chip learning via in-memory computing and RRAM	A. Dhar, D. Chen	UIUC
30	NeuroSim: A circuit-level benchmark simulator for neuro-inspired architectures	P.-Y. Chen, S. Yu	ASU
31	Neural learning through spike-timing dependent plasticity of Dzyaloshinskii domain walls	A. Sengupta, A. Banerjee, K. Roy	Purdue