Workshop on Hardware and Algorithms for Learning On-a-chip (HALO) 2015

http://nimo.asu.edu/halo

Time	Schedule
8:00am – 8:15am	Introduction and opening remarks
8:15am – 8:50am	**Keynote talk**: Jason Cong (UCLA): *Machine Learning on FPGAs*
Session 1: Hardware Acceleration of Machine Learning Session Chair: Jae-sun Seo (ASU)	
8:50am – 9:15am	Eugenio Culurciello (Purdue): *Deep Learning in Practice*
9:15am – 9:40am	Eric Chung (Microsoft): *Toward Accelerating Deep Learning at Scale Using Specialized Hardware in the Datacenter*
9:40am – 10:05am	Jian Li (Huawei): *System Optimization of Symbiotic Data Management in Cognitive Computing Cloud*
10:05am – 10:30am	Yasuki Tanabe (Toshiba): *Design of Heterogeneous Multi-core SoCs for Image Recognition and an Architecture for Deep Convolutional Networks*
10:30am – 10:45am	Coffee Break
Session 2: Frontiers of Learning Algorithms Session Chair: Wenyao Xu (SUNY Buffalo)	
10:45am – 11:10am	Hector Valdez (Raytheon): *Hierarchical Deep ATR*
11:10am – 11:35am	Peter Chin (Draper Lab): *Applications of Deep Networks - from Github to Brain*
11:35am – 12:00pm	Jeff Schneider (Uber): *Machine Learning Algorithms I Wish We Had in Hardware*
12:00pm – 1:30pm	Lunch
Session 3: Frontiers of Hardware Design Session Chair: Dhireesha Kudithipudi (RIT)	
1:30pm – 1:55pm	Andrew Cassidy (IBM): *The TrueNorth Neurosynaptic Processor: Cognitive Computing at Low-Power, Real-Time, and Large-Scale*
1:55pm – 2:20pm	Emre Neftci (UCI): *Neuromorphic Learning Machines*
2:20pm – 2:45pm	Damien Querlioz (CNRS): *Revisiting Memory for Neuroinspired Systems*
Poster Session	
2:45pm – 3:50pm	Poster presentations (2mins each)
3:50pm – 4:30pm	Poster discussions
4:30pm – 5:00pm	Workshop summary